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QUERY CONTROL FORM			RTIS USE ONLY	
Application No.	09/767,582	Prepared by	J. Robbins	Tracking Number 05869902
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JACKET			
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

SPECIFICATION

a. Page Missing
b. Text Continuity
c. Holes through Data
d. Other Missing Text
e. Illegible Text
f. Duplicate Text
g. Brief Description
h. Sequence Listing
i. Appendix
j. Amendments
k. Other

CLAIMS

a. Claim(s) Missing
b. Improper Dependency
c. Duplicate Numbers
d. Incorrect Numbering
e. Index Disagrees
f. Punctuation
g. Amendments
h. Bracketing
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j. Duplicate Text
k. Other

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Thank You

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RESPONSE see attached

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rather than in the plane of the substrate (which would be the x- and y-axes).

For the sake of visual simplicity, the structure of the active substrate has only been shown schematically with the understanding that the basic layer structure is the same as that shown in previous embodiments, and that the active substrate may be constructed with the previously described construction steps. In addition, the relative sizes of the active components to the chip and pads are not to scale. The VCSEL and photodetector (PD) are shown larger than in constructed configurations. An exemplary detailed structure of the IC chip layer and exemplary constructions steps are provided below.

Instead of joining IC chip layer **350** to active substrate **320** with a layer of anisotropic conductive material, one may use an adhesive bonding sheet. In order to join the electrical pads **332** of layer **350** to the pads **332** of substrate **320**, holes are made through the bonding sheet (such as by pre-punching) in the locations of the pads, and conductive bonding material is disposed on one set of pads. Substrate **320** and layer **350** are then laminated together with heat and mild pressure. One may also use the multilayer lamination process described in U.S. patent Application Serial No. 09/192,003, filed November 13, 1998, entitled *"Multilayer Laminated Substrates with High Density Interconnects and Methods of Making the Same,"* assigned to the assignee of the present application, and invented by Messrs. Hunt Jiang, Tom Massingill, Mark McCormack, and Michael Lee. In addition, one may also use the gas-less solder paste described in U.S. patent Application Serial No. 09/203,126, filed December 1, 1998, entitled *"Conductive Composition,"* assigned to the assignee of the present application, and invented by Messrs. Mark McCormack, Hunt Jiang, Solomon Beilin, Albert Chan, and Yasuhito Takahashi for the conductive bonding material used in the holes of the bonding sheet. (For diffusion bonding of two metal pads together in a Z-connection, the method newly invented by Messrs. Kuo-Chuan Liu and Michael G. Lee and described in yet to be filed patent application serial No. 10/066,485, entitled *"Transient Liquid Alloy Bonding,"* (TBL) and assigned to the assignee of the present application, appears to be useful in the structures of the present application.) The Z-axis connection of pads **332** can also be

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